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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/666,742
Filing Date: September 19, 2003
Appellant(s): WOOD ET AL.

Brick G. Power
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed March 10, 2008 appealing from the Office action mailed October 10, 2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,354,695	LEEDY	10-1994
6,524,881	TANDY et al	2-2003

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 70-74, 76-86 and 88-98 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leedy et al (US 5,869,354) in view of Grigg (US 6,562,661) and Tandy et al (US 6,524,881).

Claims 70 and dependent Claims thereof generally require a method for thinning a semiconductor substrate comprising molding a support structure on an active surface of the semiconductor substrate; removing material from a back side of the semiconductor substrate to form a thinned semiconductor substrate; and transporting the thinned substrate for further processing. Claims 82 and dependent Claims thereof generally require a method for thinning a semiconductor substrate comprising forming a support structure on an active surface of the semiconductor substrate; securing the semiconductor substrate to a platen with the active surface facing the platen and the support structure abutting at least one surface or feature of or on the platen; removing material from a back side of the semiconductor substrate supported by the support structure and the platen to form a thinned semiconductor substrate; and transporting the thinned substrate for further processing.

Leedy et al disclose a method of making a dielectrically isolated integrated circuit. Leedy et al disclose the step of attaching an annular support ring to an edge portion of a semiconductor substrate on a principal side, and thinning the backside of the semiconductor substrate, as required by present claims 70-74 and 82-86. See column 7, line 50 to column 8, line 15, column 44, lines 35-50 and column 45, lines 1-5. Leedy et al also discloses the use of a package as required by present Claim 73 and

85. See the Abstract and Figures 16A –16B. As Leedy et al disclose multiple chip modules, in other words the need for further processing the thinned substrate, and therefore the limitation "transporting the thinned semiconductor substrate for further processing" is met. See Figures 32A-C for example.

However, Leedy et al does not disclose forming a layer comprising unconsolidated material over at least an outer peripheral portion of the active surface; and at least partially consolidating the unconsolidated material within at least outer peripheral regions of the layer; and forming the support structure by molding or using the platen as required by the afore mentioned Claims.

Grigg disclose stiffeners for connective structures that are configured to be secured to a semiconductor device component such as a semiconductor die or substrate by a tape automated bonding process. See the Abstract. Grigg et al disclose forming a layer comprising unconsolidated material over at least an outer peripheral portion of the active surface; and at least partially consolidating the unconsolidated material within at least outer peripheral regions of the layer, as required in present Claims 74, 83-86 and 88. See Figure 6, column 7, lines 50-60 and column 16, lines 1-15. Moreover, Grigg et al disclose energy beams as required in Claims 89-90. Furthermore, Grigg et al disclose stereolithographically forming the structure as required by present Claims 91. See column 12, line 55 to column 13, line 60.

Tandy et al disclose a method for marking a semiconductor die, which has an application in a thinning process. See Abstract. Tandy et al disclose that it is known in the art to mold support structures and it is known to use a platen 56 to provide physical

support for a wafer during a backgrinding process. See Figure 1A and 2, and column 5, lines 25-40. Support structure 58, is below platen 56, and wafer 10 is on the platen, with the active side of the wafer down. The backside of the wafer, top portion is ground by 52. See Figure 2.

It would have been obvious for one of ordinary skill in the art, at the time of the invention, to bond the interconnect circuit membrane as disclosed by Leedy et al using the stiffeners as disclosed by Grigg, for their known benefit in fabricating connective structures and to arrive at the presently claimed invention. The use of a known bonding process to fabricate interconnect circuit membranes which are known in the prior art, is *prima facie* obvious. Moreover, it would have been obvious for one of ordinary skill in the art, at the time of the invention, to mold a support structure and provide a platen in a process as disclosed by Leedy et al and Grigg , for their known benefit in the art of forming support structures and providing physical support, respectively, as disclosed by the Tandy et al reference. As Tandy et al also pertains to supporting and/or thinning wafers, a *prima facie* case of obviousness is established. Therefore, the presently claimed limitations are obvious in view of the cited references.

(10) Response to Argument

Appellants argue that the Examiner has erred in at least one respect: no apparent reason has been provided as to why one of ordinary skill in the art would have combined teachings from Leedy et al, Grigg and Tandy et al to provide a process in

which a support structure is molded onto on an active surface of a semiconductor substrate. The Examiner maintains that proper motivation to combine the references has been provided, as it would have been obvious for one of ordinary skill in the art, at the time of the invention to mold a support structure as disclosed by Leedy et al, using the molding process of Tandy, for its known benefit in the art of forming support structures. Moreover, the Examiner notes as Tandy et al also pertains to supporting and/or thinning wafers, a *prima facie* case of obviousness is established. The cited prior art discloses that it is known to use molding to form support structures. The use of a known method, molding, to provide a structure which is known in the prior art, a support for a wafer, would have been obvious to one of ordinary skill in the art at the time of the invention.

Appellants further argue that claim 70 is drawn to a process that requires "molding a support structure on an active surface of a semiconductor substrate", and since none of Leedy et al, Grigg or Tandy et al teaches or suggests a process that includes molding, there would have been no apparent reason for one of ordinary skill in the art to combine teachings from these references to develop a method in which a support structure is molded. The Examiner maintains that Tandy et al disclose that it is known in the art to mold support structures (use of a molding compound). See column 5, lines 35-37. Moreover, the Examiner further notes that Leedy et al discloses forming the support by using epoxy bonding techniques, which can be considered molding as it involves the application of pressure to a polymer. See column 9, line 10.

Appellants further argue that without the benefit of hindsight provided by the present application there would be no apparent reason for one of ordinary skill in the art to combine teachings from Leedy et al , Grigg and Tandy et al in such a way as to render obvious the subject matter recited in independent claim 70, nor has the Examiner provided a convincing line of reasoning as to why one of ordinary skill in the art would have had any apparent reason to combine teachings from these reference in the manner that has been asserted. The Examiner maintains that the cited prior art discloses the formation of a support structure by molding and therefore the use of a known process, molding, to form a known device, a semiconductor support, would have been obvious to one of ordinary skill in the art. The rationale for one of ordinary skill in the art to form a support by molding is provided by the cited prior art which discloses the use of a molding process for the benefit of forming semiconductor supports.

Appellants argue that it has been asserted that all of the references pertain to making semiconductors in the on page 7 of the Final Office Action mailed 10/10/2007, and that the afore mentioned assertion overlooks the fact that making semiconductors is a broad field that includes a large number of separate distinct processes that employ different techniques. The Appellants argue that in combining the teachings of Leedy et al, Grigg and Tandy et al the Examiner has attempted to combine teachings from separate fields within the general field of making semiconductors; thinning; the manufacture of flexible carrier substrates; and wafer marking. The Examiner maintains that there is no reason why one of ordinary skill in the art would be limited to a particular aspect of manufacturing semiconductors, such as for example thinning semiconductors.

Moreover, the Examiner notes that both Leedy et al and Tandy et al describe thinning semiconductors.

Appellants further argue that the teachings of Leedy et al, Grigg and Tandy et al do not support a *prima facie* case of obviousness, since none of the references teaches or suggest molding a support structure. As discussed above, the Examiner maintains that Tandy et al disclose that it is known in the art to mold support structures (use of a molding compound). See column 5, lines 35-37. Moreover, the Examiner further notes that Leedy et al disclose forming the support by using epoxy bonding techniques, which can be considered molding as it involves the application of pressure to a polymer. See column 9, line 10. Furthermore, would have been obvious for one of ordinary skill in the art, at the time of the invention, to mold a support structure in a process as disclosed by Leedy et al and Grigg , for its known benefit in the art of forming support structures as disclosed by the Tandy et al reference. As Tandy et al and Leedy et al pertain to supporting and thinning wafers, a *prima facie* case of obviousness is established.

Appellants cite *KSR int'L Co v. Teleflex*, 82 USPQ 2d 1396 (2007) to support the argument that a claim "is not proved obvious merely by demonstrating that each of its elements was independently, known in the prior art" and that there must also be "an apparent reason to combine the known elements in the fashion claimed by the patent at issue". The Examiner maintains that as required by *KSR Int'l Co. V. Teleflex Inc., supra* , the prior art references teach all of the claimed elements, with the difference between being that a separate reference discloses molding a support for semiconductors to be used during the thinning of a wafer. The rationale for combining the references, as

required by *KSR Int'l Co. V. Teleflex Inc., supra* is that the use of a known method, molding, to form a known structure, the support, is no more "than the predictable use of prior art elements according to their established functions":

With respect to Claim 82, Appellants argue that frame 18 is on the backside of the substrate. The Examiner agrees, and notes that bonding frame or ring 19 is on the top side of the substrate. Appellants further argue that while Leedy et al teaches a separate bonding frame or ring 19 may be secured to an active surface of the substrate, the teachings of Leedy et al are limited to securing the bonding frame after the substrate 10 has been thinned, and cites column 8, lines 48-52. The Examiner notes that there is no such limitation as to when the bonding frame or ring is attached in Leedy et al.

Grigg as noted by Appellants are not relied upon to disclose limitations pertaining to the support or platen.

With respect to the teachings of Tandy et al, Appellants argue that Tandy et al does not teach or suggest that a support structure of any type is secured to the front of the wafer 10, between the wafer 10 and the platen 56, during the backgrinding process. The Examiner maintains that Tandy et al disclose a support structure (17) secured to the front of the wafer 10, between the wafer 10 and the platen 56, during the backgrinding process. See Figure 2, support 17, and column 5, lines 35-40.

Appellants argue that since none of Leedy et al, Grigg or Tandy et al identify any shortcomings with the wafer thinning processes of Leedy and Tandy, one of ordinary skill in the art wouldn't have had any apparent reason to combine the teachings of the

references. The Examiner maintains that individual references do not have to identify specific problems in order to establish a *prima facie* case of obviousness.

Appellants cite *KSR Int'L Co v. Teleflex*, 82 USPQ 2d 1396 (2007) to support the argument that a claim "is not proved obvious merely by demonstrating that each of its elements was independently, known in the prior art" and that there must also be "an apparent reason to combine the known elements in the fashion claimed by the patent at issue". The Examiner maintains that as required by *KSR Int'l Co. V. Teleflex Inc., supra* , the prior art references teach all of the claimed elements, with the difference between being that a separate reference discloses a platen as a support for semiconductors to be used during the thinning of a wafer. The rationale for combining the references, as required by *KSR Int'l Co. V. Teleflex Inc., supra* is that the use of a known device, a platen, for its known purpose, as a support, is no more "than the predictable use of prior art elements according to their established functions":

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

ALEXANDER G. GHYKA

PRIMARY EXAMINER AU 2812

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